Over-design Methodology for Operating Voltage Minimization

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Agenda

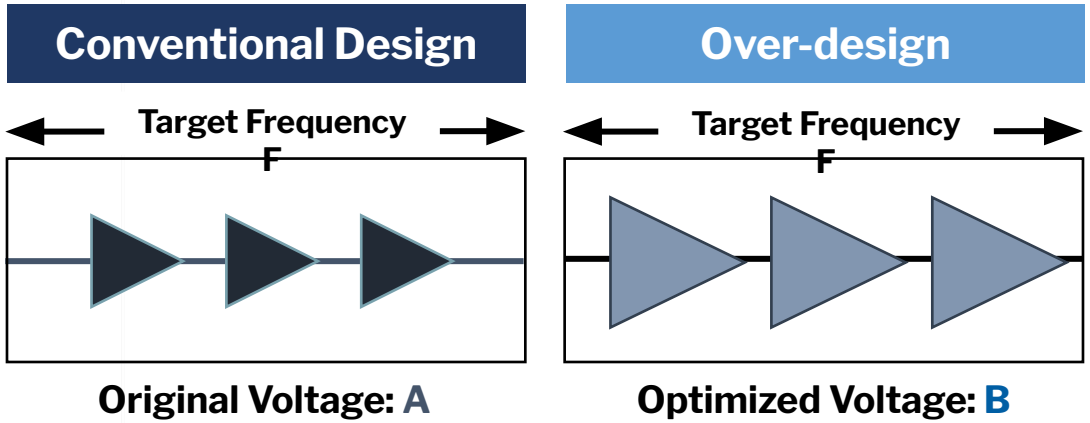
- Motivation
- Methodology Concept
- Proposed Design Methodology
- Experimental Results
- Summary

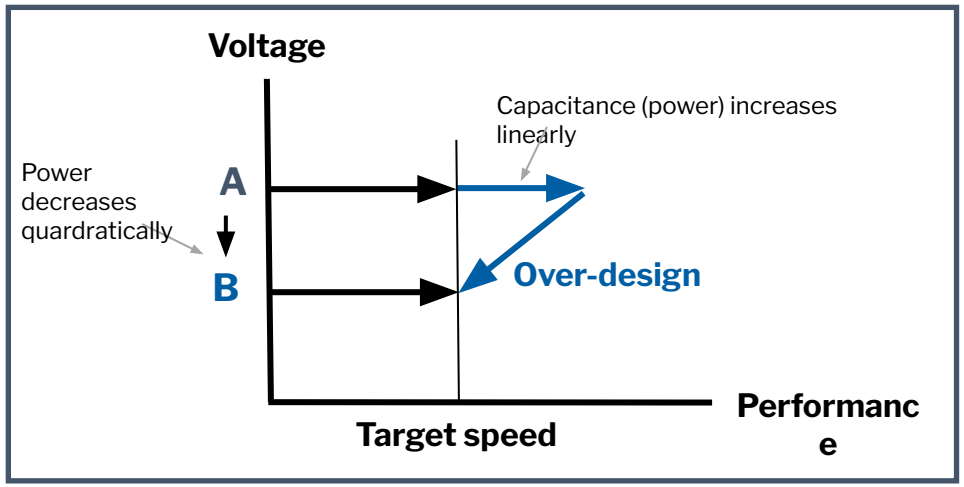
Motivation

- **Power, one of the most important parameters of electronic devices**
  - Both leakage and dynamic power are important
  - Various techniques (power-gating, multiple threshold, multiple gate length, etc.) are adopted to reduce leakage power
  - Multiple voltages, dynamic voltage-frequency scaling, various clock/data-gating techniques can reduce dynamic power
  - Lowering voltage can reduce dynamic power quadratically. However, in sub-10nm advanced process technologies, supply voltage is stuck at around 0.75V
- **Can we further reduce the level of supply voltage?**
  - Cell sizing affects capacitance linearly □ power changes linearly
  - Timing optimization at lower voltage increases capacitance linearly
  - Lowered voltage decreases power quadratically
  - Design at lower voltage can reduce power while meeting target speed, compensating linear power increased from over-sizing

Methodology Concept

- **Over-design with voltage lowering**
  - Conventional design methodology is to achieve target speed exactly
  - Over-design methodology is to achieve more than the required speed
  - Reducing supply voltage of the over-designed chip as low as possible while satisfying the original target speed, can reduce dynamic power further than conventional methods
  - In the example below, “Over-design” with voltage “B” can have lower power than the “Conventional Design” with voltage “A”





Proposed Design Methodology

- **Voltage Optimization Flow***

Over-design at nominal voltage ≒ Exact-design at lower voltage
We find the lowest voltage satisfying the target speed!

1. Prepare two libraries characterized with two different voltage corners
2. Do conventional P&R flow until clock tree synthesis
3. Reduce voltage
4. Calculate delay at the lower voltage (from interpolation between the two libraries)
5. Optimize design as much as possible to meet the original target speed (OrigFreq)
6. If the target speed cannot be met, increase voltage until the speed target is met

- Place_opt and CTS are done at original voltage
- Voltage opt settings are introduced after CTS and before clock opt stage

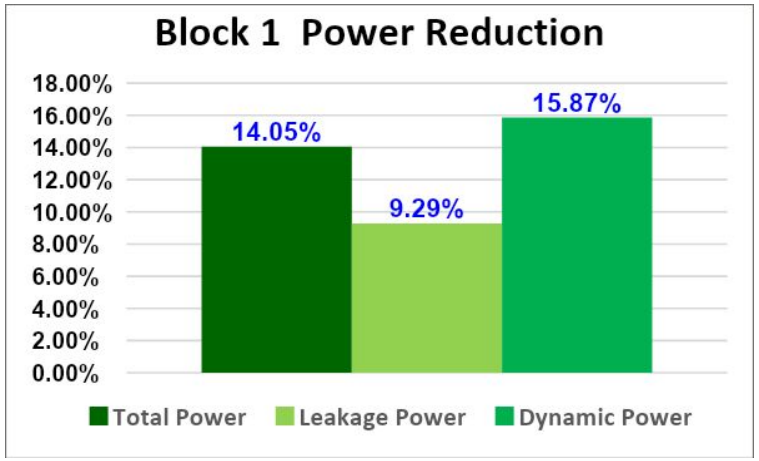
- Voltage opt flow starts here
- Scaling lib group after sanity checks need to be sourced
- Voltage opt range and targets need to be set
- Voltage_opt is a stand alone command to be used after clock_opt

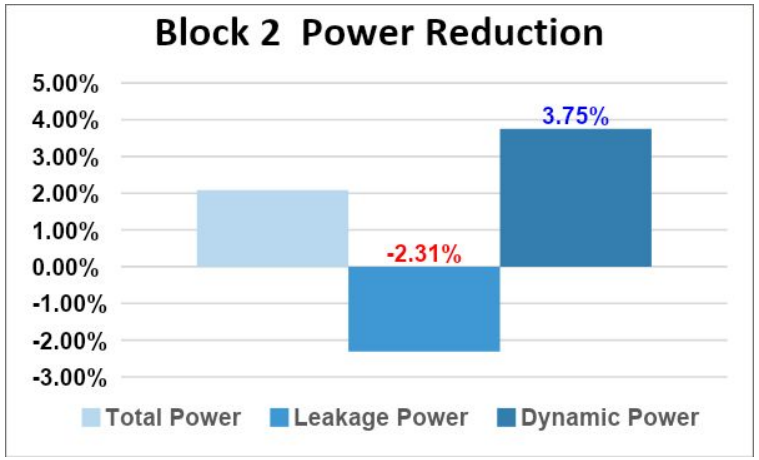
- Route and Route_opt are run at the voltage optimized from voltage opt command

* Synopsys IC-Compiler2

Experimental Results

- **Experimental 1: SSD Controller with Samsung 5nm Technology**
  - Block 1: voltage can be reduced from 0.675V to 0.621V
    - **15.87%** dynamic power reduction while meeting the original target speed
  - Block 2: voltage can be reduced from 0.675V to 0.6513V
    - Block 2 is more difficult to meet target speed than Block 1
    - **3.75%** dynamic power reduction satisfying the original target speed
    - But, leakage power increases by 2.31% because of increasing LVT portion
  - The minimum voltage can be different for each block in a chip





Experimental Results

- **Experimental 2: CPU core with Samsung 4nm Technology**
  - Target speed: 1.2GHz @ 0.675V
  - Conventional design: voltage can be reduced from 0.675V to 0.6075V
    - **18.49%** dynamic power reduction
  - Over-design: **1.6GHz @ 0.675V -> 1.2GHz @ 0.585V**
    - Voltage can be lower than the conventional design (0.6075V -> 0.585V)
    - **20.66%** dynamic power reduction satisfying the original target speed
    - However, leakage power is higher than that of the conventional design because of increasing LVT portion
    - Apply to products that is important to dynamic power

Voltage range setting option

-effort low	range 3% to –base_voltage
-effort med	range 5% to –base_voltage
-effort high	range 8% to –base_voltage
-effort ultra_high	range 12% to –base_voltage
-low_voltage -high_voltage	user-defined

Case	Option	voltage[V]	R2R Setup [ns]				Power [mW]						LVT [%]	Cell area	Util (%)
			WNS	TNS	NVP	Freq	Leakage	Change	Dynamic	Change	Total	Change			
Conventional Design	Reference	0.6750	0	0	3	1205	9.38E-01		5.66E+01		5.75E+01		11.65	14528.82	63.53%
	low	0.6547	-0.01	0	6	1190	9.74E-01	3.83%	5.27E+01	-6.88%	5.37E+01	-6.70%	14.98	14364.26	62.83%
	med	0.6413	-0.01	0	3	1190	1.04E+00	10.59%	5.08E+01	-10.25%	5.18E+01	-9.91%	17.60	14548.72	63.61%
	high	0.6210	-0.02	-0.1	24	1176	1.18E+00	26.34%	4.81E+01	-14.97%	4.93E+01	-14.29%	23.18	14932.13	65.25%
	ultra-high	0.6075	-0.05	-1	112	1136	1.39E+00	48.71%	4.61E+01	-18.49%	4.75E+01	-17.39%	30.90	14983.67	65.47%
Over-design	user-defined	0.5850	-0.03	-1.6	350	1163	1.67E+00	77.92%	4.49E+01	-20.66%	4.66E+01	-19.05%	35.07	16788.48	71.48%

Summary

- **What is over-design methodology?**
  - Low power technique that can reduce dynamic power by reducing the supply voltage as low as possible while satisfying target performance
- **Voltage optimization flow is useful for low power design**
  - Proposed methodology was verified with industry 5/4nm technology
- **Future Work**
  - Need verification of the accuracy of scaled (interpolated) libraries
  - Need detailed implementation design methodology including separation of voltage domains, level-shifters insertion, etc.
  - Need for silicon validation

Thank you